

REMARKS

This is intended as a full and complete response to the Office Action dated June 19, 2003, having a shortened statutory period for response set to expire on September 19, 2003. Please reconsider the claims pending in the application for reasons discussed below.

Claims 1-38 remain pending in the application and are shown above. Claims 1-38 are rejected. Reconsideration of the rejected claims is requested for reasons presented below.

Claims 1, 3, and 37 are amended to clarify the invention. Claim 4 is amended to correct matters of form. Applicant submits that the changes made herein do not introduce new matter.

Claims 1, 2, 9, 12, and 15 stand rejected under 35 U.S.C. § 102(b) as being anticipated by *Taguchi, et al.* (U.S. Patent No. 5,308,793). Applicant has amended claim 1 to specify that the first barrier layer is selected from the group consisting of $TiSi_xN$, $TiN(C)$, $TiNSi(C)$, Ta , TaC , $TaN(C)$, $TaNSi(C)$, W , WN_x , SiO_xN_y , SiC , AlN , and Al_2O_3 . *Taguchi, et al.* describes a process in which a first barrier layer of SiN_x is deposited on a substrate to protect the sidewalls of the substrate from moisture and oxidation during later processing steps. *Taguchi, et al.* provides SiN_x as an alternative to barrier layers for aluminum such as Ti barrier layers that can experience oxidation (column 2, lines 19-28) during later processing steps. *Taguchi, et al.* only teaches SiN_x as having the appropriate properties to protect the substrate (column 2, lines 36-52). *Taguchi, et al.* does not teach or suggest depositing $TiSi_xN$, $TiN(C)$, $TiNSi(C)$, Ta , TaC , $TaN(C)$, $TaNSi(C)$, W , WN_x , SiO_xN_y , SiC , AlN , or Al_2O_3 as a first barrier layer. Applicant respectfully requests withdrawal of the rejection of claim 1, and of claims 2, 9, 12, and 15, which depend thereon.

Claims 3, 4, 16, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787). *Taguchi, et al.* describes a process in which a first barrier layer of SiN_x is deposited on a substrate and then etched before a second barrier layer of Ti, TiN, WSi, or polysilicon is deposited on the substrate. *Zhao, et al.* describes a process in which an aperture 15 is formed in a dielectric layer 12, wherein the aperture extends to a barrier layer 13 of TiN

(for an aluminum feature) or TiN, TiW, Ta, TaN, or WN (for a copper feature) (column 5, lines 22-27). A second barrier layer 16 of SiN or SiON (column 5, lines 53-58) is then deposited on the substrate. Applicant submits that the combination of *Taguchi, et al.* and *Zhao, et al.* does not teach or suggest a method of filling one or more of a via and a trench in a patterned substrate in which a first barrier layer of TiSi_xN, TiN(C), TiNSi(C), Ta, TaC, TaN(C), TaNSi(C), W, WN_x, SiO_xN_y, SiC, AlN, and Al₂O₃ is deposited in one or more of the via and the trench, as recited in amended claim 1. As *Taguchi, et al.* and *Zhao, et al.*, alone, or in combination, do not provide all of the limitations of claim 1, *Taguchi, et al.* and *Zhao, et al.* do not provide all of the limitations of claims 3, 4, 16, and 17, which depend on claim 1. Applicant respectfully requests withdrawal of the rejection of claims 3, 4, 16, and 17.

Applicant further submits that the combination of *Taguchi, et al.* and *Zhao, et al.* does not describe depositing a second barrier layer selected from the group consisting of Ta, TaN, TiSiN_x, TaSiN_x, W, and WN_x. *Taguchi, et al.* describes a second barrier layer of Ti, TiN, WSi, or polysilicon. *Zhao, et al.* describes a second barrier layer of SiN or SiON. As claims 4 and 16 specify a second barrier layer selected from the group consisting of Ta, TaN, TiSiN_x, TaSiN_x, W, and WN_x, *Taguchi, et al.* and *Zhao, et al.*, alone, or in combination, do not provide all of the limitations of claims 4 and 16. Applicant respectfully requests withdrawal of the rejection of claims 4 and 16.

Claims 5 and 6 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.*, in view of *Zhao, et al.* and further in view of *Simon, et al.* (U.S. Patent No. 5,933,753). As discussed above, Applicant submits that *Taguchi, et al.*, in view of *Zhao, et al.* does not provide all of the limitations of claim 1. Applicant further submits that *Taguchi, et al.*, in view of *Zhao, et al.* and further in view of *Simon, et al.* does not provide all of the limitations of claim 1, upon which claims 5 and 6 depend. Applicant respectfully requests withdrawal of the rejection of claims 5 and 6.

Claims 7 and 8 are rejected under U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.*, in view of *Zhao, et al.* (U.S. Patent No. 5,846,332). The Examiner states that *Taguchi, et al.* discloses the claimed invention with the exception of the first barrier layer being deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated process tool. The Examiner further

states that *Zhao, et al.* provides a chemical vapor deposition chamber that can be used for both a thermal deposition and a subsequently performed plasma process, and that it would have been obvious to use the single chamber of *Zhao, et al.*

Applicant respectfully traverses the rejection. *Zhao, et al.* describes a CVD chamber that can thermally deposit materials and then plasma treat the materials. However, *Zhao, et al.* does not teach or suggest that the CVD chamber can deposit a barrier layer and then remove the barrier layer from the horizontal surfaces of the substrate. *Taguchi, et al.*, in view of *Zhao, et al.* does not teach, show, or suggest a method of filling one or more of a via and a trench in a patterned substrate, comprising depositing a generally conformal first barrier layer in one or more of the via and the trench on the patterned substrate by chemical vapor deposition, wherein the first barrier layer is selected from the group consisting of TiSi_xN , $\text{TiN}(\text{C})$, $\text{TiNSi}(\text{C})$, Ta , TaC , $\text{TaN}(\text{C})$, $\text{TaNSi}(\text{C})$, W , WN_x , SiO_xN_y , SiC , AlN , and Al_2O_3 , removing the first barrier layer from the horizontal surfaces of the patterned substrate, depositing a second barrier layer by physical vapor deposition, and then depositing one or more conductive materials, wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool, as recited in claim 7. Applicant respectfully requests withdrawal of the rejection of claim 7 and of claim 8, which depends thereon.

Claims 10 and 13-14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Gelatos, et al.*, (U.S. Patent no. 5,391,517). As discussed above, Applicant submits that *Taguchi, et al.* does not provide all of the limitations of claim 1. Applicant further submits that *Taguchi, et al.* in view of *Gelatos, et al.* does not provide all of the limitations of claim 1. As claims 10 and 13-14 depend from claim 1, *Taguchi, et al.* in view of *Gelatos, et al.* does not provide all of the limitations of claims 10 and 13-14. Applicant respectfully requests withdrawal of the rejection of claims 10 and 13-14.

Claim 37 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Uzoh* (U.S. Patent No. 5,930,669) in view of *Taguchi, et al.* As discussed above, *Taguchi, et al.* does not teach or suggest depositing a generally conformal first barrier layer selected from the group consisting of TiSi_xN , $\text{TiN}(\text{C})$, $\text{TiNSi}(\text{C})$, Ta , TaC , $\text{TaN}(\text{C})$,

TaNSi(C), W, WN_x, SiO_xN_y, SiC, AlN, and Al₂O₃. Furthermore, *Taguchi, et al.* does not describe or suggest depositing a second barrier layer sufficient to provide a barrier on the bottom of a trench without significantly impairing conduction between the conductive material deposited in the via and a metal layer underlying the via, as *Taguchi, et al.* does not describe depositing a barrier layer on a trench.

Uzoh describes depositing a conformal barrier layer and then etching the bottom of the barrier layer such that there is no interface between metal in a underlying metal layer and metal in the via. As *Uzoh* teaches removing the barrier layer from the bottom of the via, *Uzoh* does not suggest or motivate depositing a second barrier layer sufficient to provide a barrier on the bottom of a trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer.

Thus, *Uzoh* and *Taguchi, et al.*, alone, or in combination, do not teach, show, or suggest a method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising depositing a generally conformal first barrier layer on the patterned substrate by chemical vapor deposition, wherein the first barrier layer is selected from the group consisting of TiSi_xN, TiN(C), TiNSi(C), Ta, TaC, TaN(C), TaNSi(C), W, WN_x, SiO_xN_y, SiC, AlN, and Al₂O₃, removing the first barrier layer from the horizontal surfaces of the patterned substrate, depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material deposited in the via and the metal layer, and then depositing one or more conductive materials, as recited in claim 37. Applicant respectfully requests withdrawal of the rejection of claim 37.

Claims 18-21, 26, 29, 32-34, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* (U.S. Patent No. 5,407,698). The Examiner asserts that it would have been obvious to use atomic layer deposition in the process of *Taguchi, et al.* with the barriers of *Taguchi, et al.* or *Zhao, et al.* Applicant respectfully traverses the rejection.

Emesh describes depositing an adhesion layer of TiN by sputtering followed by a thin (1000 Å) layer of W and a thick layer of W (5000 Å). *Emesh* provides specific

conditions for the deposition of tungsten, but does not teach or suggest processes for depositing other materials. *Taguchi, et al.* describes depositing a first barrier of SiN by CVD in a via. *Zhao, et al.* describes depositing a first barrier of SiN or SiON by CVD in a via. There is no suggestion or motivation in *Taguchi, et al.*, *Zhao, et al.* (U.S. Patent No. 5,674,787), or *Emesh*, alone, or in combination, to use the process *Emesh* describes for the deposition of tungsten in the process of *Taguchi, et al.* in which a first barrier of SiN is deposited by CVD and then etched before a second barrier layer is deposited. The references do not teach or motivate a process in which a first barrier layer is deposited by atomic layer deposition and then etched. Thus, *Taguchi, et al.*, *Zhao, et al.* (U.S. Patent No. 5,674,787), or *Emesh*, alone, or in combination, do not teach, show, or suggest a method of filling one or more of a via and a trench in a patterned substrate, comprising depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition, removing the first barrier layer from the horizontal surfaces of the patterned substrate, depositing a second barrier layer by physical vapor deposition, and then depositing one or more conductive materials, as recited in claim 18. Applicant respectfully requests withdrawal of the rejection of claim 18 and of claims 19-21, 26, 29, and 32-34, which depend thereon.

Applicant respectfully traverses the rejection of claim 38. As discussed above, *Taguchi, et al.*, *Zhao, et al.* (U.S. Patent No. 5,674,787), or *Emesh*, alone, or in combination, do not suggest or motivate using the process *Emesh* describes for the deposition of tungsten in the process of *Taguchi, et al.* in which a first barrier of SiN is deposited by CVD and then etched before a second barrier layer is deposited. The references do not teach or motivate a process in which a first barrier layer is deposited by atomic layer deposition and then etched. *Taguchi, et al.*, *Zhao, et al.* (U.S. Patent No. 5,674,787), or *Emesh*, alone, or in combination, do not teach, show, or suggest a method of filling one or more of a via and a trench in a patterned substrate having a metal layer underlying the via, comprising depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition, removing the first barrier layer from the horizontal surfaces of the patterned substrate, depositing by physical vapor deposition a second barrier layer sufficient to provide a barrier on the bottom of the trench without significantly impairing conduction between the conductive material

deposited in the via and the metal layer, and then depositing one or more conductive materials, as recited in claim 38. Applicant respectfully requests withdrawal of the rejection of claim 38.

Claims 22 and 23 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.*, in view of *Zhao, et al.* and *Emesh* as applied to claims 18-21 above, and further in view of *Simon, et al.* As discussed above, Applicant submits that *Taguchi, et al.*, in view of *Zhao, et al.* and *Emesh* does not provide all of the limitations of claim 18. Applicant further submits that *Simon, et al.* does not teach or suggest a process in which a first barrier layer is deposited by atomic layer deposition and then etched. Thus, *Taguchi, et al.*, in view of *Zhao, et al.* and *Emesh* and further in view of *Simon, et al.* does not provide all of the limitations of claim 18, upon which claims 22 and 23 depend. Applicant respectfully requests withdrawal of the rejection of claims 22 and 23.

Claims 24 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* and further in view of *Zhao, et al.* (U.S. Patent No. 5,846,332). The Examiner asserts that it would have been obvious to use the CVD chamber of *Zhao, et al.* (U.S. Patent No. 5,846,332) with the process of *Taguchi, et al.* modified in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh*. Applicant respectfully traverses the rejection.

Zhao, et al. (U.S. Patent No. 5,846,332) describes a CVD chamber that can perform plasma processes. However, *Zhao, et al.* (U.S. Patent No. 5,846,332) does not describe an atomic layer deposition chamber, or a process in which a barrier layer is deposited and etched in an atomic layer deposition chamber. Moreover, *Zhao, et al.* in combination with *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* does not describe or suggest a process in which a barrier layer is deposited and etched in an atomic layer deposition chamber. Thus, *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* and further in view of *Zhao, et al.* (U.S. Patent No. 5,846,332) does not teach, show, or suggest a method of filling one or more of a via and a trench in a patterned substrate, comprising depositing a generally conformal first barrier layer on the patterned substrate by atomic layer deposition, removing the first barrier layer from the horizontal surfaces of the patterned substrate,

wherein the first barrier layer is deposited and removed from the horizontal surfaces of the patterned substrate within a single chamber of an integrated processing tool, depositing a second barrier layer by physical vapor deposition, and then depositing one or more conductive materials, as recited in claim 24. Applicant respectfully requests withdrawal of the rejection of claim 24, and of claim 25, which depends thereon.

Claims 27-28 and 30-31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* and further in view of *Gelatos, et al.* As discussed above, Applicant submits that *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* does not provide all of the limitations of claim 18. Applicant further submits that *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* and further in view of *Gelatos, et al.* does not provide all of the limitations of claim 18. As claims 27-28 and 30-31 depend from claim 18, *Taguchi, et al.* in view of *Zhao, et al.* (U.S. Patent No. 5,674,787) and *Emesh* and further in view of *Gelatos, et al.* does not provide all of the limitations of claims 27-28 and 30-31. Applicant respectfully requests withdrawal of the rejection of claims 27-28 and 30-31.

Claim 35 is rejected under 35 U.S.C. § 103(a) as being unpatentable over *Taguchi, et al.* in view of *Cronin* (U.S. Patent No. 5,818,110). The Examiner states that it would have been obvious to use an etch stop layer underlying the first barrier layer in order to protect the underlying conductive region in the invention of *Taguchi, et al.* as *Cronin* teaches, and to remove it in order to allow an electrical connection to the conductive region. Applicant respectfully traverses the rejection.

Cronin describes depositing a conformal layer of parylene over an aperture of a substrate, removing the parylene from the horizontal surfaces of the substrate, removing an etch stop from the bottom of the aperture, and filling the aperture with metal (column 6, lines 10-40, Figures 12-16). There is no suggestion or motivation in *Cronin* to deposit a second barrier layer after the etch stop is removed, as *Cronin* teaches that the parylene is selectively removed where electrical contact with the metal line is desired (column 6, lines 22-23).

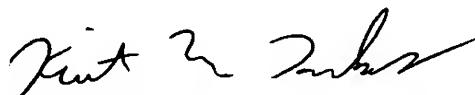
Taguchi, et al. describes depositing a first barrier layer of SiN, etching the bottom of the first barrier layer, and then depositing a second barrier layer. The embodiments

shown in Fig. 2a-2d, Fig. 12, 13a-13c, 14a-14c of *Taguchi, et al.* do not include an etch stop. However, Figures 8-11 of *Taguchi, et al.* show an embodiment in which SiN barrier layer is deposited and then etched from the bottom of the via which has an underlying TiSi layer that serves as an etch stop. *Taguchi, et al.* does not teach or suggest removing the underlying TiSi layer from the bottom of the via. A Ti layer 23 is then deposited on the intact etch stop. Thus, Applicant submits that there is no motivation or suggestion to combine *Taguchi, et al.*, which describes a process in which two barrier layers are deposited in an aperture, wherein an etch stop in the aperture is not removed, and the bottom of the aperture is left covered by the second barrier layer, with *Cronin*, which describes depositing one barrier layer, and then removing the barrier and an etch stop from the bottom of the aperture to leave the bottom of the aperture exposed. Applicant respectfully requests withdrawal of the rejection of claim 35.

In conclusion, the references cited by the Examiner, alone or in combination, do not teach, show, or suggest the invention as claimed.

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully request that the claims be allowed.

Respectfully submitted,



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